REMARKS

Claims 1-6, 8-13, and 15-18 stand rejected under 35 USC §103(a) as being unpatentable over Tsujikawa et al., U.S. patent publication US2002/0014849 in view of Garringer et al., U.S. patent 4,377,843. Claims 7 and 14 stand rejected under 35 USC §103(a) as being unpatentable over Tsujikawa et al., U.S. patent publication US2002/0014849 in view of Garringer et al., U.S. patent 4,377,843 and further Taguchi, U.S. patent publication US2003/0052250.

Reconsideration and allowance of each of the pending claims 1-18 is respectfully requested.

Tsujikawa et al., U.S. patent publication US2002/0014849 discloses that to make compatible low consumption power formation of a control circuit of a light emitting element and high frequency formation of operational frequency band and constituting a variety of usable combination elements of light emitting elements and light receiving elements, bias current is provided to a current mirror for dividing monitor current of a photodiode PD1 by a current source to thereby compensate drive function of a post stage in driving thereof by low current. Reference voltage of a current-voltage conversion portion 4 is set in accordance with an input range of an operational amplifier 51 of a gain adjusting portion 5 at a post stage and input to the operational amplifier 51 is fitted to an input range optimizing amplifying function. A variation of frequency band or phase is restrained by adjusting gain by using a differential amplifier 53 of the gain adjusting portion 5. There are provided switching circuits SW1 and SW2 for selectively supplying monitor current from two photodiodes to respective APC loops of laser diodes

LD1 and LD2 to thereby deal with a 2LD-1PD element and two of 1LD-1PD elements. The circuit includes driver circuits 1 and 2 that supply drive current to laser diodes LD1 and LD2 to thereby make the laser diodes LD1 and LD2 emit light. A current mirror portion 3 is provided with two current mirrors CM1 and CM2. An input terminal IN1 of the current mirror CM1 is connected to the photodiode PD1 for dividing monitor current IPD1 in two and outputting thereof from output terminals OUT1 and OUT2. The current mirror CM2 is for controlling two 1LD-1PD elements. The operational amplifier 55 receives the reference voltage via a resistor at the positive phase input and the output voltages and the reference voltage are calculated and amplified and outputted to an error amplifier 6. Output voltages of the output terminal OUT10 and the inverted output terminal OUT11 are provided to a negative phase input and a positive phase input of the operational amplifier 56 respectively via resistors, the operational amplifier 56 receives the reference voltage at the positive phase input via a resistor and the output voltages and the reference voltage are calculated and amplified and outputted to an error amplifier 7. The error amplifiers 6 and 7 compare the output voltages outputted from the operational amplifiers 55 and 56 with reference voltages, when the output voltage is lower than the reference voltage, a logical level of the output is determined as "L" and when the output voltage is higher than the reference voltage, the logical level is determined as "H". Sample hold control circuits 8 and 9 are provided with up/down counters, not illustrated, carry out upcounting or downcounting in accordance with logical levels of the outputs of the error amplifiers 6 and 7 when there is brought about an enable state and hold count values when there is brought about a disable state. The

driver circuits 1 and 2 generate drive current ILD1 and ILD2 in accordance with the count values of the SH control circuits 8 and 9.

Garringer et al., U.S. patent 4,377,843 discloses a microprocessor-based circuit for interfacing between a plurality of serial data terminals and an external parallel data operating system. The interface circuit includes an asynchronous receiver-transmitter, which converts serial data to parallel data and converts parallel data to serial data. The interface circuit multiplexes received serial data from the terminals and couples that serial data to the receiver-transmitter. The microprocessor in the interface circuit further controls the transfer of this now-parallel data to the external parallel data operating system. The microprocessor also controls the transfer of parallel data from the parallel data operating system, which is converted to serial data by the asynchronous receiver-transmitter, demultiplexed by the interface circuit and transmitted to the terminals. Both the transmission and the reception of serial data is coordinated by the microprocessor, which also controls the receiver-transmitter and a set of registers connected to the operating system on a parallel data bus. A typical driver is schematically shown as device 46 within the block for the tri-state driver circuit 42.

Taguchi, U.S. patent publication US2003/0052250 discloses a laser-driving device including a high-frequency current generating circuit generating a high-frequency current superimposed on a control current output from a light intensity control circuit for light intensity control, and supplied to a laser diode as a drive current, the high-frequency current generating circuit has a sourcing current source, a sinking

current source, current switches connected between the current sources and a drive output terminal respectively, a gated oscillation circuit oscillating with a desired frequency, and switch drive circuits complementarily on/off controlling the current switches by using a drive switching signal obtained by removing a high-frequency component from an output signal of the oscillation circuit. The high-frequency current generating circuit can increase the amplitude of the high-frequency current superimposed on the control current of the laser diode and which generates less heat while suppressing power consumption. The semiconductor device consists of a laser diode 1, a light-monitoring detector 2 for monitoring light intensity, a current-to-voltage conversion resistor 3, an APC (auto-power control) circuit 4, a high-frequency blocking filter 5 and a high-frequency current generating circuit 10.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record.

In accordance with features of the preferred embodiment of the present invention, an optical margin testing system for automatic power control loops provides effective performance and is simple to implement. In the optical margin testing system for automatic power control loops the operating point of the light emitting device are both increased and decreased by a set percentage threshold to validate signal integrity margins. The margin testing is implemented without requiring complex software control or readjusting any bias control potentiometers. Optical margin testing system of the preferred embodiment effectively implements a 2-bit switched current source into an APC loop so that when the appropriate control signal is provided, the bias generator

can increase or decrease the operating point by a defined percentage X%. A single I/O using a tri-state receiver where the three states are normal mode, +X% mode, and -X% mode provides the control signal.

Independent claim 1 recites an optical margin testing system for an automatic power control loop comprising: an optical circuit including a laser diode and a monitor diode coupled to said automatic power control loop; a bias generator circuit for generating a control signal; said control signal applied to said automatic power control loop; and said control signal enabling an operation point of said laser diode to both increase and decrease by a set percentage value. Applicants respectfully submit that the subject matter of the present invention as recited by independent claim 1 is not shown nor suggested by the references of record including Tsujikawa et al., Garringer et al., and Taguchi. A bias generator circuit for generating a control signal; said control signal applied to said automatic power control loop; and said control signal enabling an operation point of said laser diode to both increase and decrease by a set percentage value, as claimed in independent claim 1 is not shown nor suggested by Tsujikawa et al., and Garringer et al. Applicants respectfully submit that Taguchi adds nothing to render obvious the subject matter of the present invention as recited by independent claim 1. Thus, independent claim 1 is patentable.

Independent claim 12 further defines the invention reciting optical margin testing system for an automatic power control loop comprising: an optical circuit including a laser diode and a monitor diode coupled to said automatic power control loop; a tri-state receiver; a current mirror coupled to said tri-state receiver for generating

a control signal; said control signal applied to said automatic power control loop; said control signal enabling an operation point of said laser diode to both increase and decrease by a set percentage value; and an input signal being applied to said tri-state receiver for selecting one of a normal operational mode, an increased set percentage value operational mode, and a decreased set percentage value operational mode. Applicants respectfully submit that the subject matter of the present invention as recited by independent claim 12 is not shown nor suggested by the references of record including Tsujikawa et al., Garringer et al., and Taguchi. Applicants respectfully submit that independent claim 12 is patentable for the same reasons as independent claim 1. Applicants respectfully submit that the references of record including Tsujikawa et al., Garringer et al., and Taguchi fail to teach or suggest the use of a tri-state receiver for generating a control signal; said control signal applied to said automatic power control loop as recited by independent claim 12.

Dependent claims 2-11 and 13-18 further define the invention of patentable claims 1 and 12 and are likewise patentable.

Reconsideration and allowance of each of the pending claims 1-18 is respectfully requested.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-18 is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application,

the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

By: _____

Joan Pennington
Reg. No. 30,885
Telephone: (312) 670-0736